Electronic Version
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Claims

[c1] 1. A stack chip package structure, comprising:
a carrier with a carrier surface and a plurality of bonding pads, wherein the bonding pads are set up on the carrier surface;
a die with an active surface and a back surface, wherein the back surface of the die is in contact with the carrier surface of the carrier and the active surface of the die has a plurality of metal pads thereon;
an adhesive layer on the active surface of the die;
a thermal conductive block with a bonding surface for attaching to the active surface of the die through the adhesive layer, wherein the bonding surface includes a central surface and a plurality of peripheral surfaces surrounding the central surface, wherein the peripheral surfaces are further away from the active surface of the die than the central surface relatively, and that the peripheral surfaces and the central surface are on non-coplanar planes;
a plurality of conductive wires electrically connecting each metal pad to a corresponding bonding pad; and
a molding compound enclosing the die, the thermal conductive block and the conductive wires.

[c2] 2. The stack chip package structure of claim 1, wherein the peripheral surfaces are ladder, sloping or curved surfaces.

[c3] 3. The stack chip package structure of claim 1, wherein thickness of the adhesive layer between the peripheral surface and the active surface of the die is greater than the adhesive layer between the central surface and the active surface of the die.

[c4] 4. The stack chip package structure of claim 1, wherein the carrier is a substrate or a lead-frame.

[c5] 5. The carrier is a lead-frame in claim 4 including:
a die pad for stacking over sequentially a die and a thermal conductive block.; and
a plurality of leads having a bonding pad on one end of the leads for attaching a conductive wire.

[c6] 6. The stack chip package structure of claim 1, wherein the thermal conductive block is a dummy die, a metal block or a graphite block.

[c7] 7. A stack chip package structure, comprising:
a die with an active surface, wherein the active surface has a plurality of metal pads thereon;
an adhesive layer on the active surface of the die;

a thermal conductive block with a bonding surface for attaching to the active surface of the die through the adhesive layer, wherein the bonding surface further includes a central surface and a plurality of peripheral surfaces surrounding the central surface, wherein the peripheral surfaces are further away from the active surface of the die than the central surface relatively, and that the peripheral surfaces and the central surface are on non-coplanar planes;

a plurality of leads, wherein each end of the lead is connected to a corresponding metal pad; and

a molding compound for enclosing a portion of the die, the thermal conductive block and a portion of the leads.

[c8] 8. The stack chip package structure of claim 7, wherein the peripheral surfaces are ladder, sloping or curved surfaces.

[c9] 9. The stack chip package structure of claim 7, wherein the molding compound exposes the back surface of the die.

[c10] 10. The stack chip package structure of claim 7, wherein thickness of the adhesive layer between the peripheral surface and the active surface is greater than the adhesive layer between the central surface and the active surface.

[c11] 11. The stack chip package structure of claim 7, wherein the thermal conductive block is a dummy die, a metal block or a graphite block.

[c12] 12. A stack chip package structure, comprising:
a die with a first surface;
an adhesive layer on the first surface of the die; and
a stack structure with a bonding surface for attaching to the first surface of the die, wherein the bonding surface further includes a central surface and a plurality of peripheral surfaces surrounding the central surface, wherein the peripheral surfaces are further away from the active surface of the die than the central surface relatively, and that the peripheral surfaces and the central surface are on non-coplanar planes.

[c13] 13. The stack chip package structure of claim 12, wherein the peripheral surfaces are ladder, sloping or curved surfaces.

[c14] 14. The stack chip package structure of claim 12, wherein thickness of the adhesive layer between the peripheral surface and the active surface of the die is greater than the adhesive layer between the central surface and the active surface of the die.

[c15] 15. The stack chip package structure of claim 12,

wherein the stack structure includes a dummy die.

[c16] 16. The stack chip package structure of claim 12, wherein the stack structure includes a thermal conductive block.

[c17] 17. The stack chip package structure of claim 12, wherein the stack structure includes a functional die.

[c18] 18. The stack chip package structure of claim 12, wherein the first surface of the die has a plurality of metal pads and the stack chip package structure further includes:

a carrier with a carrier surface and a plurality of bonding pads, wherein the bonding pads are set up on the carrier surface and a second surface of the die is attached to the carrier surface of the carrier;

a plurality of conductive wires for connecting each metal pad with a corresponding bonding pad electrically; and

a molding compound for enclosing the die, the stack structure and the conductive wires.

[c19] 19. The stack chip package structure of claim 18, wherein the carrier is a substrate or a lead-frame.